Notice of Allowability	Application No.	Applicant(s)	
	09/741,802	KIMURA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Interview Summary on 04/07/07 and 01/24/08*.

2. ☐ The allowed claim(s) is/are _____.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

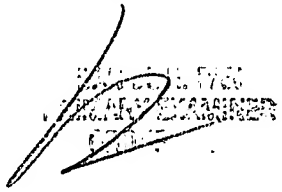
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *attached* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.



Continuation of Attachment(s) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 06/18/07,12/19/06, 11/27/06.

Reasons for Allowance/Examiner's Amendment

None of the prior art of record teaches the details of the combined features of the specific application instruction operating unit, the rewritable register, the processor core and the control unit (claim 6); the exception processing during the execution of the first application specific instruction and before the second instruction interrupt according the read mode, the setting of value indicating the exception in register or a flag, the exception process for the first instruction before the second instruction interrupt upon occurrence of the exception according to the reading of the register or the flag and returning from interruption caused by second instruction by performing the interrupt processing for the second instruction (claim 15); determining before executing the exception processing for the first application specific instruction and before the second instruction interrupt processing whether to perform the exception processing by checking a value stored in a first register or a flag associated with the second instruction causing the interruption, indicating the processor to perform the exception, setting the exception indicating the exception in a second register or second flag, performing the exception for the first instruction upon occurrence of the exception according to reading of the second register or the second flag and returning from interruption caused by the second instruction by performing the interrupt by second instruction (claim 17); the specific application purpose operation instruction , the

operation exception detection flag, the flag control unit in validating the operation exception flag, the interrupt control unit, the operation exception detection flag invalidate instruction (claims 20,21); The he operation exception detection flag, the specific application purpose instruction, the flag control unit, the control unit for controlling the generation of the interruption, when the interrupt control unit has received a notice that interrupt is generated, and when the flag control unit has received operation exception detection flag write instruction, and the writing of the flag value into the operation exception detection flag for setting valid (claim 22); the operation exception detection flag, the condition code register, specific application purpose instruction, the flag control unit, the branch/interrupt return instruction control unit, and the interrupt control unit for controlling the generation of the interrupt when interrupt control unit has received a generated interrupt notice (Claim 24).

Authorization for this examiner's amendment was given in a telephone interview with Mehdi Sheikerz on 01/22/08.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Please **AMEND** claims 6, 15, 17, 20, 21, 22 and 24 according to the following

1. (CANCELLED)

2. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, wherein said specific application-purpose instruction operating unit is built in as an intellectual property of an ASIC (Application Specific Integrated Circuit).

3. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, wherein the number of cycles control to issue the same succeeding instructions.

4. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, further comprising:

a rewritable register provided within a processor core of the processing apparatus, wherein

said rewritable register prescribes a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to use a result thereof, and said issuing of the instruction is controlled based on said number of cycles.

5. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 6, further comprising:

a rewritable register provided within a processor core of the processing apparatus, wherein

said rewritable register prescribes a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is the same as the instruction of said specific application-purpose instruction operation unit, and said issuing of the same instruction in succession is controlled based on said number of cycles.

6. (CURRENTLY AMENDED) An information processing apparatus, comprising:

a control unit to process an operation instruction, which does not have a functional specification, as a specific application-purpose operation instruction;

a specific application-purpose instruction operating unit supporting flexible pipeline processing and carrying an operation of the specific application-purpose operation instruction for each application field;

a rewritable register prescribing a number of cycles from when an instruction of said specific application-purpose instruction operating unit is issued until issuance of an immediately subsequent instruction that is same as the instruction of said specific application-purpose instruction operation unit, wherein the instruction of said specific application-purpose instruction operating unit occupies an operating unit source; and

a processor core including a flag changing over between a case where a number of cycles, which is prescribed from when an instruction of said specific application-purpose instruction operating unit is issued until issuance of the same instruction in succession, becomes the same as another number of cycles, which is prescribed from when the instruction of the specific application-purpose instruction operating unit is issued a result of the specific application-purpose instruction operating unit is obtained, and a case where the same instruction is issued in succession in each cycle,

wherein said control unit controls issuing the instructions based upon the rewritable register and the processor core flag.

7-12 (CANCELLED)

13. (PREVIOUSLY PRESENTED) The exception processing method according to claim 15, further comprising:

determining before the execution of the execution processing, whether to perform the exception processing by checking whether the second instruction causing the interruption is a specific application-purpose operation instruction.

14. (CANCELLED)

15. (CURRENTLY AMENDED) An exception processing method for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of an interrupt processing for the second instruction, an exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction, the exception processing method comprising:

performing the exception processing for the exception during the execution of the first instruction and before the second instruction interrupt processing, according to a read operation mode indicating to the processor whether to perform the exception processing;

setting, when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception in a register or a flag;

determining when the interruption is caused by the second instruction, whether the exception has occurred by reading the register or the flag value;

performing the exception processing for the first instruction before the second instruction interrupt processing, upon occurrence of the exception according to the reading of the register or the flag value and returning from the interruption caused by the second instruction by performing the interrupt processing for the second instruction.

16. (CANCELLED)

17. (CURRENTLY AMENDED) An exception processing method for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of an interrupt

processing for the second instruction, an exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction, the exception processing method comprising:

determining before executing the exception processing for the first instruction and before the second instruction interrupt processing, whether to perform the exception processing by checking whether a value, which is stored in a first register or a first flag and associated with the second instruction causing the interruption, indicates to the processor to perform the exception processing;

setting, when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception in a second register or a second flag;

determining when the interruption is caused by the second instruction, whether the exception has occurred by reading the second register or the second flag value;

performing the exception processing for the first instruction, upon occurrence of the exception according to the reading of the second register or the second flag value and returning from the interruption cased by the second instruction by performing the interrupt processing for the second instruction.

18. (CANCELLED)

19. (CANCELLED)

20. (CURRENTLY AMENDED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when an operation exception has been detected during an execution of a specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during an execution

of a trap instruction to generate the interruption,

wherein

said interruption control unit carries out a control relating to the generation of the interruption, when said interruption control unit has received a notice that the interruption is generated, and

when said flag control unit has received an operation exception detection flag invalidate instruction, said flag control unit invalidates said operation exception detection flag indicating an operation exception has not been detected during an execution of a specific application-purpose operation instruction.

21. (CURRENTLY AMENDED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when an operation exception has been detected during an execution of the specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during an execution of a trap instruction to generate the interruption,

wherein said interruption control unit carries out a control relating to the generation of the interruption, when said interruption control unit has received a notice that the interruption is generated, and when said flag control unit has received an operation exception detection flag read instruction, said flag control unit reads a value of said operation exception detection flag for notifying the interruption control unit.

22. (CURRENTLY AMENDED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has

been detected;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when an operation exception has been detected during an execution of the specific application-purpose operation instruction; and

a flag control unit which notifies an interruption control unit that an interruption due to the operation exception of the specific application-purpose operation instruction is to be generated, when said operation exception detection flag has been set to the valid state during an execution of a trap instruction to generate the interruption,

wherein said interruption control unit carries out a control relating to the generation of the interruption, when said interruption control unit has received a notice that the interruption is generated, and when said flag control unit has received an operation exception detection flag write instruction, said flag control unit writes a value into said operation exception detection flag for setting said operation exception detection flag to the valid state.

23. CANCELLED

24. (CURRENTLY AMENDED) An information processing apparatus having a specific application-purpose operation instruction, said information processing apparatus comprising:

an operation exception detection flag indicating whether an operation exception has been detected;

a condition code register that is set based on a value that is held in said operation exception detection flag;

a specific application-purpose operation instruction executing unit setting said operation exception detection flag to a valid state when the operation exception has been detected during an execution of the specific application-purpose operation instruction;

a flag control unit setting the condition code register based on a value that is held in said operation exception detection flag; and

a branch/interruption return instruction control unit determining whether an interruption is generated or not based on a value held in said condition code register and a value shown by an instruction field during the execution of a trap instruction to generate the interruption, and, when the interruption is to be generated, notifying an interruption control unit that the interruption due

to the operation exception of a specific application-purpose operation instruction is to be generated,

wherein said interruption control unit carries out a control relating to the generation of the interruption, when said interruption control unit has received a notice that the interruption is generated.

25. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag invalidate instruction, said flag control unit invalidates said operation exception detection flag.

26. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag read instruction, said flag control unit reads the value of said operation exception detection flag.

27. (PREVIOUSLY PRESENTED) The information processing apparatus according to claim 24, wherein

when said flag control unit receives an operation exception detection flag write instruction, said flag control unit writes the value into said operation exception detection flag.

28. (ORIGINAL) The information processing apparatus according to claim 24, wherein

said information processing apparatus has an instruction having an operational function specialized for an image processing as the specific application-purpose operation instruction.

29-32 (CANCELLED)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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